

Long-Term Reliability of Si/Si_{0.7}Ge_{0.3}/Si HBTs from Accelerated Lifetime Testing

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Abstract—Accelerated lifetime tests were performed on double-mesa structure Si/Si_{0.7}Ge_{0.3}/Si npn heterojunction bipolar transistors, grown by molecular beam epitaxy, in the temperature range of 175 °C-275 °C. The transistors (with 5x20 μm² emitter area) have DC current gains ~ 40-50 and f_T and f_{max} of up to 22 GHz and 25 GHz, respectively. It is found that a gradual degradation in these devices is caused by the recombination enhanced impurity diffusion (REID) of boron atoms from the p-type base region and the associated formation of parasitic energy barriers to electron transport from the emitter to collector layers. This REID has been quantitatively modeled and explained, to the first order of approximation, and the agreement with the measured data is good. The mean time to failure (MTTF) of these devices at room temperature under 1.35 x10⁴ A/cm² current density operation is estimated from the extrapolation of the Arrhenius plots of device lifetime versus reciprocal temperature. The results of the reliability tests offer valuable feedback for SiGe heterostructure design in order to improve the long-term reliability of the devices and circuits made with them.

1. Introduction

The rapid progress of Si/SiGe heterojunction bipolar transistor (HBT) technology has made Si-based devices very attractive for microwave applications. Among the existing SiGe technologies, Si/SiGe/Si HBTs have been most widely studied [1]-[5] owing to the advantage in material characteristics, such as the near-zero conduction band offset between Si and strained SiGe layers, which is preferred for npn HBT applications. The use of a smaller bandgap SiGe alloy in the base of the HBT increases the efficiency of minority carrier injection. This results in an increase of collector current and current gain even though the base doping is high. The high base doping yields a smaller base resistance, which in turn leads to high maximum oscillation frequency f_{max}, high Early voltage and low noise figure. However, the p-n junctions in a HBT must be well defined and coincident with the heterojunctions. Base dopant outdiffusion during epitaxy and/or during device processing and operation shifts

the location of p-n junctions, usually resulting in the formation of parasitic energy barriers near the base-emitter and base-collector junctions, which can significantly reduce the current gain and cutoff frequency [6], [7].

Device performance is a function of time in general, since the device performance parameters are liable to change, gradually or abruptly, as the operation time accumulates. Therefore, excellent performance observed during the initial measurement on a device does not necessarily guarantee long-term reliability. For the Si/SiGe HBT technology to be a choice for commercial radio frequency integrated circuits the long-term reliability of Si/SiGe HBTs has to be proven and, to our knowledge, very limited report on this subject exists in the literature. Neugroschel *et al* [8] have investigated the time-to-failure of GeSi bipolar transistors with current-acceleration method in which base-emitter reverse-bias stress was applied at room temperature. While this method can significantly accelerate the degradation of devices and is effective for observing the device degradation caused by hot carriers, it is not suitable for evaluating the

device degradation caused by atomic diffusion. Another investigation, on the effects of base-emitter reverse-bias stress on the cryogenic operation of SiGe HBTs, has been reported by Babcock *et al* [9]. Specially tailored techniques are required to evaluate the long-term reliability of devices since it takes impractically long times to observe any appreciable degradation in the device performance under normal operating conditions. The long-term reliability can be most effectively evaluated by accelerated lifetime testing (ALT), i.e., measuring the device lifetime at elevated temperatures under normal bias conditions [10]-[12]. Unlike the current-acceleration method used by Neugroschel *et al* [8], this ALT method resembles the real operating condition of HBTs. By extrapolating the HBT lifetimes at high temperatures from the Arrhenius plot, the mean time to failure (MTTF) of the device at room temperature can be estimated. The extrapolation is based on the assumption that the degradation mechanism remains unchanged over the entire temperature range of testing and the same activation energy applies. The common sources of device degradation are diffusion of dopants, dielectric breakdown, surface or interface ion migration, metal contact degradation, electromigration of metal lines, etc. In particular, boron outdiffusion is one of the major concerns in the context of thermal budget in the fabrication and operation of SiGe/Si HBT, as it leads to the degradation of critical device parameters as mentioned above [7]. The accelerated lifetime test can be used as an effective tool to identify the source of degradation. Additionally, analysis of the failure mechanism can offer valuable feedback on the design of device structures for long-term reliability of the devices and circuits.

In this study, it has been found that forward-bias electrical-thermal stress can induce boron-outdiffusion and associated degradation for double-mesa structure npn Si/SiGe HBTs. The degradation behavior has been quantitatively modeled, to the first order of approximation. The device failure mechanism has been analyzed and its impact on device heterostructure design for improvement

of long-term reliability is discussed. In what follows, the experimental techniques are described in Section 2. The experimental results will be presented and analyzed in Section 3. The REID model based on low-level injection theory is presented in Section 4 and the important results are summarized in Section 5.

2. Experimental techniques

The HBTs used in this testing are grown by solid-source MBE. The devices (Fig. 1) have a 30 nm boron doped $\text{Si}_{0.7}\text{Ge}_{0.3}$ base layer with two undoped $\text{Si}_{0.7}\text{Ge}_{0.3}$ spacers of thickness 5 nm on each side of it. Antimony was used to dope the emitter and collector layers. The epitaxial heterostructures are fabricated into mesa type devices with $5 \times 20 \mu\text{m}^2$ emitter size, using standard photolithography and wet and dry etching techniques. Details of these procedures have been described in Ref.13. The schematic cross-section of a finished HBT is shown in Fig. 2. The measurement setup used for the lifetime test is briefly described. The device under test (DUT) was placed on a temperature-controlled hotplate and biased with collector-emitter voltage V_{CE} and base current I_{B} in the common-emitter configuration. V_{CE} , supplied by a Keithley 230 voltage source, was fixed at 3 V, while I_{B} , supplied by a Keithley 220 current source, was feedback-controlled by computer to maintain a constant collector current I_{C} of 13.5 mA, which corresponds to a current density J_{C} of $1.35 \times 10^4 \text{ A/cm}^2$ and dissipated DC power P_{diss} of 40.5 mW. It is necessary to maintain a constant collector current level, which can vary with a fixed base current due to the possible degradation of the current gain during the test, in order to keep a constant electrical stress condition throughout the entire duration of each test run. A HP2378A multimeter was included to monitor the collector current levels so that the base current could be adjusted by feedback-control in case of deviation from the acceptable range. The multimeter was also used to display the actual

Emitter cap	Si	n+	Sb	$5 \times 10^{19} \text{ cm}^{-3}$	200 nm
Emitter	Si	n	Sb	$1 \times 10^{18} \text{ cm}^{-3}$	100 nm
Spacer	$\text{Si}_{1-x}\text{Ge}_x$	i			5 nm
Base	$\text{Si}_{1-x}\text{Ge}_x$	p+	B	$6 \times 10^{19} \text{ cm}^{-3}$	30 nm
Spacer	$\text{Si}_{1-x}\text{Ge}_x$	i			5 nm
Collector	Si	n-	Sb	$2 \times 10^{16} \text{ cm}^{-3}$	250 nm
Sub-collector	Si	n+	As	$2 \times 10^{19} \text{ cm}^{-3}$	1500 nm
Substrate	Si(100)	p-		$1 \times 10^{12} \text{ cm}^{-3}$	540 μm

Figure 1: Schematic of Si/SiGe HBT, in which the As-doped subcollector layer is grown by CVD and the rest of the heterostructure is grown by MBE.

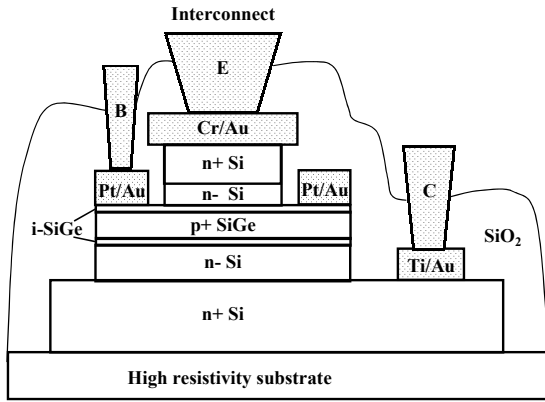


Figure 2: Schematic cross-section of a double mesa self-aligned Si/SiGe HBT.

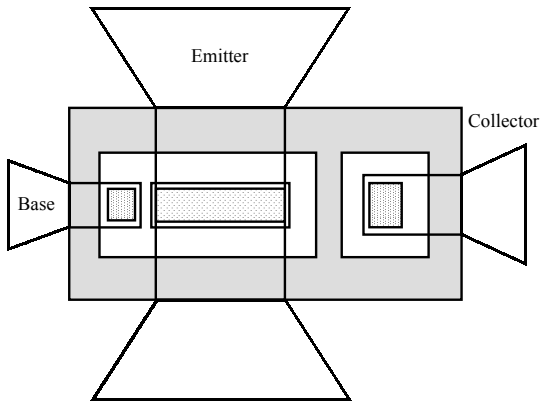


Figure 3: Layout of the tested double-mesa type single-finger Si/SiGe/Si HBTs with emitter area of $5 \times 20 \mu\text{m}^2$ and no encapsulation layer on the top of interconnection lines.

value of V_{CE} applied to the devices. The test was performed without any interruption, the bias being applied to the devices continuously till they stopped operating. Post-stress measurements were then made. Identical devices on the same wafer, which were only subjected to thermal stress without any electrical stress during each test run are classified as control devices and post-stress measurements were also performed on these devices. The lifetime tests were performed for several different hotplate temperatures, ranging from 175 °C to 275 °C. The corresponding junction temperatures, T_j , equal to 189 °C and 289 °C, respectively, and all temperatures in between were calculated by the expression,

$$T_j = P_{diss} R_{th} + T_{amb} \quad (1)$$

where P_{diss} is the power dissipation, R_{th} is the thermal resistance, and T_{amb} is the ambient temperature. The thermal resistance of the test device was extracted by the procedure outlined in Ref. 14. After V_{BE} is measured as a function of DC power dissipation with increasing V_{CE} and a fixed I_C at room temperature, V_{BE} is measured as a function of temperature with both V_{CE} and I_C fixed. The two plots are then combined and a relation between the temperature and the DC power dissipation is obtained. The slope of this plot corresponds to the thermal resistance R_{th} , which was 350 °C/W in this case. It is assumed in this calculation that the hotplate temperature is close to the junction temperature of the device, which is the case for the soft bias used in the measurements.

3. Results and analysis

It has been observed that the DC current gain, β , increases initially with time, which originates from the reduction of recombination in the base region due to the elimination of interface states and the improvement of ohmic contacts by annealing [10], [11]. After that β decreases continuously with stress time, with a faster reduction at the initial and the final

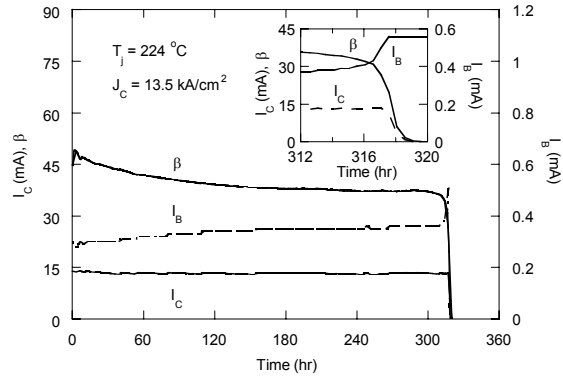


Figure 4. Typical degradation behavior for a SiGe/Si HBT.

stages than in the intermediate stage. This behavior is analyzed and discussed in Section 4. Figure 4 shows a typical degradation behavior for the tested HBTs. The constant collector current and the step-like increase of base current are manifestations of the feedback control. The apparent failure of the devices is characterized by a zero β value at the end of the tests as a result of negligible collector current after the test. The base-emitter and base-collector junction characteristics were measured after the test and compared with those measured before. The measured results for the $T_J=204^\circ\text{C}$ case are shown in Fig. 5. The reverse-biased leakage current of the base-emitter junction shows an increase after the stress test. The increase in current is also observed in the low forward bias range (below 0.7 V). An increase in leakage current across the base-emitter junction after electrical stress tests is commonly observed in both Si BJTs [15]-[18] and GaAs/AlGaAs HBTs[19]. It is believed to be caused by interface states created by hot electrons [9], [15]-[18] at the base-emitter junction sidewall. Furthermore, an extra leakage component can be present if the diode ideality factor is greater than 2. This originates from hot-electron damage at and tunneling through the dielectric layer separating the base and emitter contact regions [9]. The ideality factor of the base-emitter junction in the devices were indeed greater than 2 after the stress, and therefore the additional tunneling

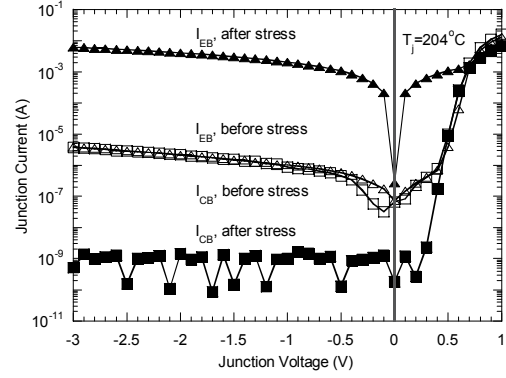


Figure 5. Base-emitter and base-collector junction diode characteristics before and after accelerated lifetime testing. Increased leakage current develops at base-emitter junction in reverse and low forward bias regimes. The reverse bias leakage current at base-collector junction is reduced.

component is expected to contribute to the total base-emitter leakage current. The reverse leakage current for the base-collector junction, on the other hand, showed a decrease after the stress was applied. This decrease is attributed to the reduction in generation current in the base-collector space charge region as a result of thermal annealing during the stress test [19]. The S-parameters were also measured before and after the test. While the device exhibited high f_T and f_{max} values before the test, these parameters could not be measured after the test, indicating that f_T and f_{max} were decreased to lower than 2 GHz, the lower frequency limit of the test equipment. The rapidly decreasing values of the measured β near the end of each testing cycle are a manifestation of the measurement technique. As described in Section 2, we have used the common-emitter biasing mode for the lifetime tests. With a decrease of DC current gain, the feedback control will increase the base current by increasing the base-emitter bias voltage V_{BE} in order to keep the collector current constant. The increase of V_{BE} will accordingly decrease the reverse bias voltage V_{CB} available to the base-collector junction, since the collector-emitter bias V_{CE} is fixed at 3 V. Decrease of V_{CB} will expedite further decrease of the current gain. As a consequence, V_{BE} will be

shifted to even higher values and it finally reaches the pre-set limit of 2 V (measured by Keithley 230 voltage source). At this point, the base current will not be changed and the degradation of DC current gain will cause the continual decrease of collector current, till it reaches a negligible value. At a higher base-collector bias, there should still be some current gain. In order to verify this measurement artifact near the end of the tests, measurements were made on the devices after the test, wherein the HBTs was biased in *common-base* mode, such that the base-emitter and base-collector biases can be varied independently. Figure 6 shows the DC current gain versus collector-base voltage of a typical device at different base-emitter bias conditions. It can be seen from this figure that if the base-emitter bias is very small, the collector current is always negligible, regardless of the base-collector bias, V_{CB} . Also, the β values are very small even at higher values of V_{BE} .

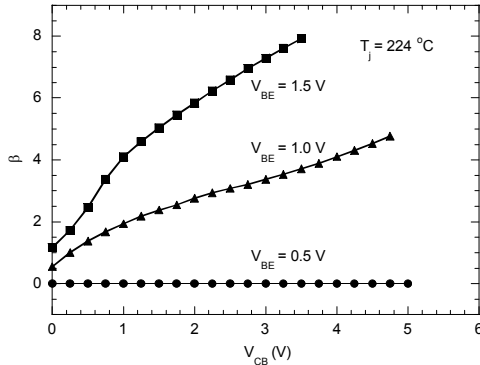


Figure 6. DC current gain versus base-collector bias voltage at different base-emitter biases after accelerated lifetime testing.

The gradual decrease of β seen in Fig. 4 is considered to be the result of boron outdiffusion and the associated formation of parasitic energy barriers [6], [7]. As boron outdiffuses from the $\text{Si}_{1-x}\text{Ge}_x$ base layer into the Si emitter and collector layers, the p-n junctions move from the Si/SiGe heterojunctions into the Si layers, which broadens the actual base width. Since Si has a wider bandgap and lower intrinsic carrier concentration than $\text{Si}_{1-x}\text{Ge}_x$, parasitic energy

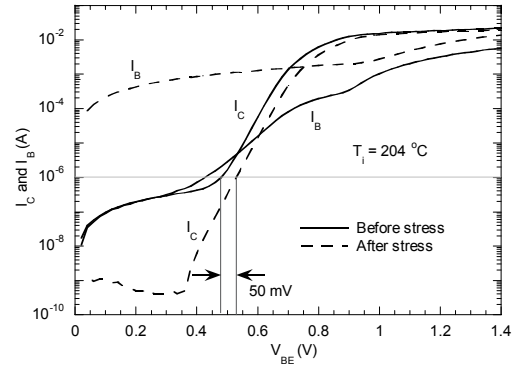


Figure 7. Gummel plots of a SiGe/Si HBT before and after accelerated lifetime testing.

barriers will be formed near the base-emitter junction and turn-on voltage of the diode should be increased [19]. Figure 7 shows the forward Gummel plots of an HBT before and after a stress test at $T_j = 204^\circ\text{C}$. In addition to the development of a base leakage current after the test, the collector current I_C profile is shifted to higher V_{BE} values, indicating the increase of device base-emitter turn-on voltage. The shift of V_{BE} was measured to be 50 mV at a collector current of $1\mu\text{A}$. The low current value avoids the effect of series resistances [19]. Similar results were obtained from the reverse Gummel plots (emitter current I_E shifted to higher V_{BC} values). The increase of the turn-on voltages can only be caused by boron outdiffusion. The Gummel plots measured on the control devices, which are only subjected to thermal stress without electrical stress, do not show the increase of turn-on voltage. The testing temperatures (up to 289°C) are too low to induce thermally activated boron diffusion. The current gain measured on the control device for each test run shows negligible change after prolonged thermal stressing. It has been reported that electromigration (EM) induced compressive stress on the top of the emitter can degrade the dc current gain β for current densities of $1 \times 10^6 \text{ A/cm}^2$ or higher [20]. In this study, the interconnect metal is not encapsulated (Fig.3) and the current density is about two orders of magnitude lower than the reported values [20]. In addition, the β degradation behavior observed in this experiment (Fig.4) is different from that caused

by compressive stress in the reported Si-based devices [20]. The distinct behavior observed in EM induced β degradation is a double minimum in the value of β with increasing stress (or time) [20]. However, this trend was not observed in this study, in spite of data being recorded at time intervals of 30 minutes. We therefore believe that the EM induced β degradation mechanism is not operative in these devices.

Defining 50% β degradation as the failure criteria, the MTTF was found to be 1.9×10^7 hours with an activation energy of 0.77 eV. The Arrhenius plot of the lifetimes versus reciprocal of test temperatures is shown in Fig. 8.

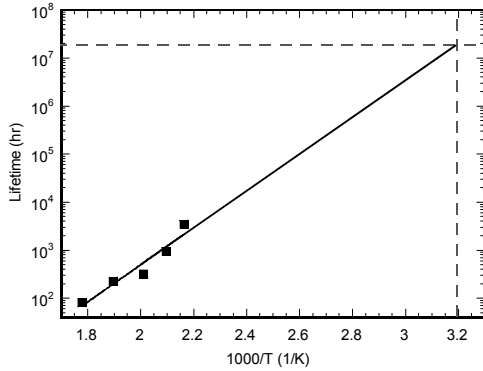


Figure 8. Arrhenius plot for lifetime of the Si/SiGe/Si HBTs. MTTF(300K)= 1.9×10^7 hours, $\Phi=0.77$ eV.

4. REID model for gradual degradation

Since boron outdiffusion occurs during the testing, a further step was taken to analyze the outdiffusion-related gradual degradation behavior with a simple diffusion model as outlined below. All the analysis is based on low-level injection theory, since the base-emitter bias during the gradual β degradation is about 0.6-0.7 V.

In a npn SiGe HBT, the collector current density J_C , assuming absence of hot-electron effects, can be expressed as [21]:

$$J_C = q \left(\int_0^{W_B} \frac{p(x)}{n_i^2(x) D_n(x)} dx \right)^{-1} e^{\frac{qV_{BE}}{kT}} \quad (2)$$

where W_B is the neutral base width, V_{BE} is the base-emitter voltage, $p(x)$ is the base doping, $D_n(x)$ is the minority carrier diffusion coefficient and $n_i(x)$ is the intrinsic carrier concentration of SiGe base, respectively. Assuming that the base current is generated only by hole injection from base into emitter, it

is modeled as [22] $J_B = J_{B0} e^{\frac{qV_{BE}}{kT}}$ and the analytical current gain takes the form:

$$\beta = \frac{J_C}{J_B} = \frac{q}{J_{B0}} \left(\int_0^{W_B} \frac{p(x)}{n_i^2(x) D_n(x)} dx \right)^{-1} \quad (3)$$

For simplicity, it is assumed the germanium and boron profiles in the base region are box-like, as shown in Fig. 9. Therefore, expanding the integral in Eq. 3 to include the out-diffused regions, we get,

$$\beta = \frac{q}{J_{B0}} \left(\int_{-W_E}^0 \frac{p(x)}{n_i^2(x) D_n(x)} dx + \int_0^{W_B} \frac{p(x)}{n_i^2(x) D_n(x)} dx + \int_{W_B}^{W_B+W_C} \frac{p(x)}{n_i^2(x) D_n(x)} dx \right)^{-1} \quad (4)$$

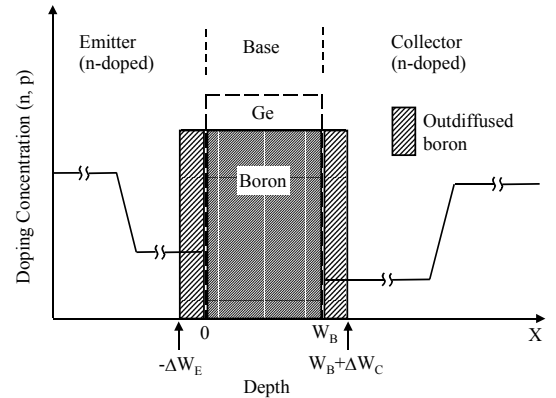


Figure 9. Model for boron outdiffusion from base layers into adjacent emitter and collector layers due to electrical-thermal stress.

where ΔW_E and ΔW_C are outdiffused region widths, as shown in Fig. 9. In this analysis it is assumed that the dopant atoms are fully ionized, i.e., $p(x)=N_A$, over the base and out-diffused regions and the diffusion coefficient $D_n(x)$ is also constant over this region. If the parasitic energy barriers caused by the boron atom outdiffusion from base to both emitter and

collector regions are ΔE_b^e and ΔE_b^c , respectively, Eq. (3) can be rewritten as:

$$\beta = \frac{qD_n n_i^2 (\text{SiGe})}{W_B J_{B0} N_A} \left(1 + \frac{\Delta W_E}{W_B} e^{\frac{\Delta E_b^e}{kT}} + \frac{\Delta W_C}{W_B} e^{\frac{\Delta E_b^c}{kT}} \right)^{-1} \quad (5)$$

Assuming that no boron outdiffusion has occurred at the onset of accelerated lifetime testing, then $\beta = \beta_0 = \frac{qD_n n_i^2 (\text{SiGe})}{W_B J_{B0} N_A}$ at $t = 0$,

and therefore the normalized current gain degradation due to outdiffusion-induced base width broadening can be expressed as

$$\frac{\beta}{\beta_0} = \left(1 + \frac{\Delta W_E}{W_B} e^{\frac{\Delta E_b^e}{kT}} + \frac{\Delta W_C}{W_B} e^{\frac{\Delta E_b^c}{kT}} \right)^{-1} \quad (6)$$

This equation is used to analyze the measured degradation of current gain β with stress time. In this work it is assumed that $\Delta W_E = \Delta W_C = \Delta L = \sqrt{D_s t}$, where D_s is the effective boron diffusion constant and t is the stress time. Thus the desired $\beta(t)$ relation is obtained. D_s can be expressed as [23]

$$D_s = D_i^{(0)} + D_i^{(+)} \frac{p}{n_i} e^{\frac{E_A}{kT}} \quad (7)$$

where $D_i^{(0)}$ and $D_i^{(+)}$ are the diffusion coefficients of boron-neutral-point-defect pairs and of boron-positively-charged-point-defect pairs, respectively. E_A is a bandgap and doping related activation energy. Originally, values of $D_i^{(0)}$ and $D_i^{(+)}$ at our testing temperatures were extrapolated from those obtained in the literature [24] in this analysis. However, it is noted here that the diffusion coefficient, $D_i^{(+)}$, is enhanced by a factor of 10^6 under bias conditions. Similar results were reported in the reliability tests of Be doped GaAs Esaki tunnel diodes [25]. The values of ΔE_b^e and ΔE_b^c are computed from the changes in Fermi levels produced by the boron outdiffusion. The decrease in the $\text{Si}_{1-x}\text{Ge}_x$ bandgap, ΔE_g , with composition is calculated from [26], [27], $\Delta E_g = 0.85x$. Finally, it is important to note that the heavy doping level in the base and out-diffused regions will cause bandgap narrowing,

which can be approximately expressed by the empirical equation [28], [29],

$$\Delta E_g^d = E_0 \ln \left(\frac{N_A}{N_1} \right), \text{ where } E_0 = 18 \text{ meV and } N_1 = 10^{17} \text{ cm}^{-3}.$$

The calculated variation of current gain with stress time is shown in Fig. 10 alongside measured data for several stress temperatures. The agreement of the calculated results at the initial and the intermediate stages of each test run is fairly good, indicating that the device degradation at each testing temperature is due to boron outdiffusion. As mentioned before, the failure at the end of a test run is defined by different processes.

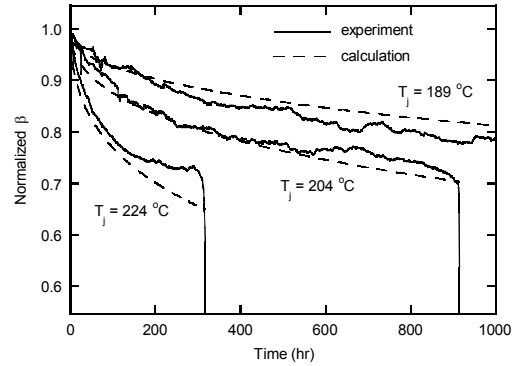


Figure 10. Measured (solid lines) and calculated (dashed lines) normalized current gain of Si/SiGe/Si HBTs as a function of stress time for different junction temperatures.

In formulating the diffusion model described above and utilizing it to analyze our data, it was found that the diffusion coefficient of boron-positively-charged-point-defect pairs ($D_i^{(+)}$) was enhanced by 6 orders under bias conditions. This anomalous behavior of the boron dopant is attributed to recombination-enhanced impurity diffusion (REID), which is reported in Be-doped GaAs [25]. For boron-doped npn $\text{Si}/\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ HBTs under forward active bias, electrons are injected from the emitter into the base. A fraction of the injected electrons will be captured by traps and recombination centers. The excess energy of the electrons is released non-radiatively and transferred to boron atoms, thereby enhancing their vibration and diffusivity. Because of the

high efficiency of the non-radiative energy transfer, the enhancement of boron diffusivity should be more significant than thermally activated diffusion. This explains why a control device, under the same thermal stress but without electrical stress, shows negligible DC current gain degradation. Similar results were reported from reliability tests on Be-doped GaAs/AlGaAs HBTs [19]. It is also appropriate to expect a more rapid degradation of Si/Si_{1-x}Ge_x/Si HBTs at higher stress current levels.

The reliability study offers valuable feedback to device heterostructure design. In practical applications, devices are usually driven at high current density for the purpose of obtaining high speed or high power. In order to minimize Si/Si_{1-x}Ge_x/Si HBT degradation under such operating conditions, it is imperative to reduce or eliminate recombination-enhanced dopant outdiffusion from the base. In this context, a SiGeC base region in npn Si/Si_{1-x}Ge_x/Si HBTs might perform better since it has been reported that carbon can successfully reduce boron outdiffusion at elevated temperatures [30]. A self-aligned mesa structure can reduce the parasitic base resistance. However, if the separation between emitter and base contact

regions is too small, the dielectric passivation in between may be cause for concern. In reality, a trade-off exists between HBT performance and long-term reliability issues.

5. Conclusions

A detailed study of forward-bias electrical-thermal stress induced degradation of Si_{1-x}Ge_x/Si HBTs is presented. From the extrapolation of the Arrhenius plots of device lifetime versus reciprocal temperature the mean time to failure (MTTF) of these devices at room temperature, under 1.35×10^4 A/cm² current density operation, is estimated to be 1.9×10^7 hours with activation energy of 0.77 eV. In these devices the gradual degradation and eventual failure are mainly caused by recombination enhanced boron outdiffusion from the base layer. Good agreement of the gradual degradation behavior is obtained with calculated results based on an analytical model which takes into account base dopant outdiffusion and the associated formation of parasitic energy barriers. A SiGeC base layer design will probably reduce boron outdiffusion and improve the long-term reliability of these devices.

REFERENCES

- [1] S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson and D. L. Harame, "Heterojunction bipolar transistors using Si-Ge alloys," *IEEE Trans. Electron Devices*, vol. 36, pp. 2043-2064, 1989.
- [2] B. Pejčinović, L. E. Kay, T.-W. Tang and D. H. Navon, "Numerical simulation and comparison of Si BJT's and Si_{1-x}Ge_x HBT's," *IEEE Trans. Electron Devices*, vol. 36, pp. 2129-2137, 1989.
- [3] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbé, G. J. Scilla, E. de Frésart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame and J. N. Burghartz, "75-GHz f_T SiGe-base heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 11, pp. 171-173, 1990.
- [4] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y.-C. Sun, B. S. Meyerson and T. Tice, "Si/SiGe epitaxial-base transistors-Part I: Materials, physics, and circuits," *IEEE Trans. Electron Devices*, vol. 42, pp. 455-467, 1995.
- [5] A. Schüppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher and U. K'nig, "Enhanced SiGe heterojunction bipolar transistors with 160 GHz- f_{max} ," in *IEDM Tech. Dig.*, pp. 743-746, 1995.
- [6] J. W. Slotboom, G. Streutker, A. Pruijboom and D. J. Gravesteijn, "Parasitic energy barriers in SiGe HBT's," *IEEE Electron Device Lett.*, vol. 12, pp. 486-488, 1991.
- [7] E. J. Prinz, P. M. Garone, P. V. Schwartz, X. Xiao, and J. C. Sturm, "The effects of base dopant outdiffusion and undoped Si_{1-x}Ge_x junction spacer layers in Si/Si_{1-x}Ge_x/Si heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 42-44, 1991.
- [8] A. Neugroschel, C.-T. Sah, J. M. Ford, J. Steele, R. Tang, and C. Stein, "Comparison of Time-to-Failure of GeSi and Si Bipolar Transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 211-213, 1996.

- [9] J. A. Babcock, A. J. Joseph, J. D. Cressler, and L. S. Vempati, "The effects of reverse-bias emitter-base stress on the cryogenic operation of advanced UHV/CVD Si- and SiGe-base bipolar transistors," in *1996 IEEE International Reliability Physics Proceedings. 34th Annual* (Cat. No.96CH38525), pp.294-299, 1996.
- [10] C. G. Peattie, J. D. Adams, S. L. Carrell, T. D. George, and M. H. Valek, "Elements of semiconductor-device reliability," *Proc. IEEE*, vol. 62, pp. 149-168, 1974.
- [11] F. H. Reynolds, "Thermally accelerated aging of semiconductor components," *Proc. IEEE*, vol. 62, pp. 212-222, 1974.
- [12] R. F. Haythornthwaite, A. R. Molozzi, and D. V. Sulway, "Reliability assurance of individual semiconductor components," *Proc. IEEE*, vol. 62, pp. 260-273, 1974.
- [13] J.-S. Rieh, L.-H. Lu, L. P. B. Katehi, P. Bhattacharya, E. T. Croke, G. E. Ponchak, and S. A. Alterovitz, "X- and Ku-band Amplifiers Based on Si/SiGe HBTs and Micromachined Lumped Components," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, pp. 685-694, 1998.
- [14] A. Samelis, "Analysis of the nonlinear characteristics of microwave power heterojunction bipolar transistors and optoelectronic integrated circuits," Ph.D. dissertation, The University of Michigan, Ann Arbor, 1996.
- [15] T. C. Chen, C. Kaya, M. B. Ketchen, and T. H. Ning, "Reliability analysis of self-aligned bipolar transistor under forward active current stress," *IEDM Tech. Dig.*, pp. 650-653, 1986.
- [16] D. D.-L. Tang and E. Hackbarth, "Junction degradation in bipolar transistors and the reliability imposed constraints to scaling and design," *IEEE Trans. Electron Devices*, vol. 35, pp. 2101-2107, 1988.
- [17] E. Hackbarth and D. D.-L. Tang, "Inherent and stress-induced leakage in heavily doped silicon junctions," *IEEE Trans. Electron Devices*, vol. 35, pp. 2108-2118, 1988.
- [18] R. A. Wachnik, T. J. Bucelot, and G. P. Li, "Degradation of bipolar transistors under high current stress at 300 K," *J. Appl. Phys.*, vol. 63, pp. 4734-4740, 1988.
- [19] M. E. Hafizi, L. M. Pawlowicz, L. T. Tran, D. K. Umemoto, D. C. Streit, A. K. Oki, M. E. Kim and K. H. Yen, "Reliability analysis of GaAs/AlGaAs HBT's under forward current/temperature stress," *GaAs IC Symposium*, pp. 329-332, 1990.
- [20] R. S. Hemmert, G. S. Prokop, J. R. Lloyd, P. M. Smith and G. M. Calabrese, "The relationship among electromigration, passivation thickness, and common-emitter current gain degradation within shallow junction NPN bipolar transistors," *J. Appl. Phys.*, vol. 53, pp. 4456-4462, 1982.
- [21] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid-State Electron.*, vol. 28, pp. 1101-1103, 1985.
- [22] E. J. Prinz and J. C. Sturm, "Current gain-Early voltage products in heterojunction bipolar transistors with nonuniform base bandgaps," *IEEE Electron Device Lett.*, vol. 12, pp. 661-663, 1991.
- [23] N. Moriya, L. C. Feldman, H. S. Luftman, C. A. King, J. Bevk and B. Freer, "Boron diffusion in Strained Si_{1-x}Ge_x epitaxial layers," *Phys. Rev. Lett.*, vol. 71, pp. 883-886, 1993.
- [24] P. Kuo, J. L. Hoyt, J. F. Gibbons, J. E. Turner, R. D. Jacowitz and T. I. Kamins, "Comparison of boron diffusion in Si and strained Si_{1-x}Ge_x epitaxial layers," *Appl. Phys. Lett.*, vol. 62, pp. 612-614, 1993.
- [25] M. Uematsu, and K. Wada, "Recombination-enhanced impurity diffusion in Be-doped GaAs," *Appl. Phys. Lett.*, vol. 58, pp. 2015-2017, 1991.
- [26] C. G. Van de Walle, R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B* vol. 34, pp. 5621-5634, 1986.
- [27] J. C. Bean, "Silicon-based semiconductor heterostructures: Column IV bandgap engineering," *Proc. IEEE*, vol. 80, pp. 571-587, 1992.
- [28] J. W. Slotboom and H. C. de Graaff, "Measurements of bandgap narrowing in Si bipolar transistors," *Solid State Electron.* vol. 19, pp. 857-862, 1976.
- [29] J. B. Kuo and T. C. Lu, "A fully analytical partitioned-charge-based model for linearly-graded SiGe-base heterojunction bipolar transistors," *Solid State Electron.* vol. 37, pp. 1561-1566, 1994.
- [30] L. D. Lanzerotti, J. C. Sturm, E. Stach, R. Hull, T. Buyuklimanli and C. Magee, "Suppression of boron transient enhanced diffusion in SiGe heterojunction bipolar transistors by carbon incorporation," *Appl. Phys. Lett.*, vol. 70, pp. 3125-3127, 1997.